We claim:

1. A process for manufacturing a power device comprising:

providing a semiconductor substrate;

growing epitaxially a first semiconductor layer of a first conductivity over a free surface of said semiconductor substrate;

forming a mask over a free surface of said first semiconductor layer, said mask including a plurality of windows exposing portions of said semiconductor layer, and being capable of blocking implants;

performing a series of implants through said implant windows to form a plurality of vertically adjacent regions of a second conductivity in said first semiconductor layer below said implant windows; and

applying a diffusion drive to link said regions of said second conductivity to form vertically oriented regions of said second conductivity in said first semiconductor layer;

forming a channel region of said second conductivity above said first semiconductor layer;

forming a plurality of MOS-gated structures through said channel region;

forming conductive regions of said first conductivity adjacent each MOS-gated structure;

forming a first electrical contact on a free surface of said substrate; and

forming a second electrical contact in electrical contact with at least said conductive regions of said first conductivity;

wherein said vertically oriented regions of said second conductivity are in substantial charge balance with said first semiconductor layer.

2. A process according to claim 1, wherein said implant windows are 0.25 to 2.0 microns wide.

3. A process according to claim 1, wherein said vertically oriented regions of said second conductivity are less than 5 microns wide.

4. A process according to claim 1, wherein said channel region is formed by growing an epitaxial semiconductor layer of said second conductivity.

5. A process according to claim 1, wherein said channel region is formed by implanting dopants of said second conductivity into said epitaxial semiconductor layer.

6. A process according to claim 1, further comprising:

growing epitaxially a second semiconductor layer of said first conductivity over said first semiconductor layer of said first conductivity;

forming a second mask over a free surface of said second semiconductor layer, said second mask including a plurality of windows exposing portions of said second semiconductor layer, and being capable of blocking implants; and

performing a series of implants through said implant windows in said second mask to form a plurality of vertically adjacent regions of said second conductivity in said second semiconductor layer below said implant windows and above said vertically oriented regions of said second conductivity in said first semiconductor layer.

7. A process according to claim 6, wherein said implant windows are 0.25 to 2.0 microns wide.

8. A process according to claim 6, wherein said vertically oriented regions of said second conductivity are less than 5 microns wide.

9. A process according to claim 6, wherein said channel region is formed by growing an epitaxial semiconductor layer of said second conductivity.

10. A process according to claim 6, wherein said channel region is formed by implanting dopants of said second conductivity into said second semiconductor layer.

11. A process according to claim 1, wherein said conductive regions of said first conductivity are source regions.

12. A process according to claim 1, wherein said first electrical contact is a drain contact, and said second electrical contact is a source contact.

13. A process according to claim 1, wherein said semiconductor substrate is of first conductivity.

14. A process according to claim 1, wherein said mask is comprised of an oxide.

15. A process according to claim 1, wherein said mask is comprised of photoresist.

16. A process according to claim 1, wherein said mask is comprised of a nitride.

17. A process according to claim 1, wherein said growing of an epitaxial semiconductor layer, said forming a mask, said performing a series of implants and said applying a diffusion drive are repeated more than two times.